CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

HIGH OUTPUT HIGH EFFICIENCY LOW VOLTAGE CHARGE PUMP
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Serial No.: 09/560,121

The paragraph beginning on page 8, and line 1:

The charge pump circuit 102 further includes a first and a second secondary phase generator 220A and 220B, which receive the first and second phase signals having the high-high crossing point and generates delayed fifth and sixth phase signals similar to the first and second phase signals, having a high-high crossing point. The charge pump circuit 102 further includes first and second pre-boot caps and associated driving circuitry 230A and 230B, which receive the first and second phase signals having high-high crossing points, and third and fourth phase signals having low-low crossing points. The charge pump circuit 102 further includes a first and a second main pump capacitor and associated pre-charge circuitry 240A and 240B, which receive the delayed fifth and sixth phase signals having the high-high crossing points from the first and second secondary phase generators 220A and 220B respectively. In a typical charge cycle, during the first phase, the first main pump capacitor 240A receives the fifth delayed phase signal having high-high crossing point from the first secondary phase generator 220A and outputs a charge to a first p-channel circuitry 250A, while the second main pump capacitor 240B is getting prebooted to a predetermined booted level by the second pre-boot capacitor 230B. In the same charge cycle, during the second phase the prebooted second main pump capacitor receives the delayed sixth phase signal from the second secondary phase generator 220B and outputs the charge to a second p-channel circuitry 250B, while the first main pump capacitor 240A is getting pre-booted to the predetermined booted level by the first pre-boot circuitry 230A. This process repeats itself every charge cycle and generally hides the preboot time required to pre-boot the first and second main capacitors 240A and 240B. As a result of staggered phase generators, the pre-boot circuitry 230A and B, and p-channel output circuitry 250A and B, the charge pump circuitry 102 can operate at supply voltages less than 1.0 Volts, and run at a faster cycle time, resulting in outputting more charge for a given size of a capacitor.

Serial No.: 09/560,121

The paragraph beginning on page 8, line 28:

Figure 3A is a timing diagram illustrating generally by way of example but not by way of limitation one embodiment of portions of first and second phase signals 310 and 320 generated by first and second primary phase generators 210A and 210B respectively, that are non-overlapping and crossing around high points 315 during every phase cycle. Also, shown are the fifth and sixth phase signals 330 and 340 generated by the first and second secondary phase generators 220A and 220B respectively, that is similar to the first and second phase signals, and including a pre-determined delay 't' from the first and second phase signals respectively.

D2

Support for deleting the words "sixth and fifth" and adding the words "fifth and sixth" in the paragraph beginning on page 8, line 28 can be found in Figure 4 and in the specification on page 8, lines 1-5.

The paragraph beginning on page 10, line 20:

The first and second phase signals coming from nodes A and B also drive the second and first pre-boot capacitors 464 and 462 respectively. Whereas the third and fourth phase signals coming from nodes E and F drive the first and second pre-boot pre-charge capacitors 474 and 476 respectively. First and second pre-boot pre-charge capacitors 474 and 476 are responsible for recharging the first and second pre-boot capacitors 462 and 464. The first and second pre-boot pre-charge capacitors 474 and 476 are tied in a cross-coupled manner, such that they precharge each other through n-channel gates 478 and 480. The reason for third and fourth phase signals to be non-overlapping and crossing each other around their low points is that the gate of the first pre-boot precharge capacitor 474 should close low before the gate of second pre-boot precharge capacitor 476 goes high, otherwise the boost voltage of the second pre-boot precharge capacitor 476 would leak off through the precharge transistor 480. The gate nodes of these second and first pre-boot precharge capacitors 476 and 474 also drive the precharge transistors 468 and 469 of the pre-boot capacitors 462 and 464, respectively. Also the gate nodes of the first and second pre-boot precharge capacitors drive charge sharing transistors 465 and 471 which provide the path that charge shares the first and second pre-boot capacitors 462 and 464, to a first and second main pump capacitors 486 and 492 of a first and second main pump capacitor and associated pre-charge circuitry 240A and 240B to a pre-determined boot level. Diode transistors

D3

467, 470, 479, and 481 are there for power-up. They charge-up first and second pre-boot capacitors 462 and 464, and first and second pre-boot precharge capacitors 474 and 476 at power-up, so that they can start pumping. Diode transistors 466 and 472 clamp gates of the first and second pre-boot precharge capacitors 474 and 476 to an n-channel VT above the gates of the first and second main pump capacitors 486 and 492, respectively. This helps to limit over-voltage and puts the excess charge onto the main pump cap where it can be passed to V_{ccp}.

Support for above amendments in the paragraph beginning on page 10, line 20 can be found in Figure 4, and in the specification on page 14, lines 26-30.

The paragraph beginning on page 12 and line 15:

The diode transistors 494, 496, 499, and 500 of the first and second main pump capacitor and associated circuitry 240A and 240B are for power-up. These diode transistors 494, 496, 499, and 500 provide a starting voltage to the first and second main pump precharge capacitors 488 and 490. Transistor 497 precharges the second main pump precharge capacitor 490, and transistor 495 precharges the first main pump precharge capacitor 488. The first and second main pump precharge capacitors 488 and 490 are used to precharge the first and second main pump capacitors 486 and 492 to a second pre-determined level through precharge devices 493 and 498. The seventh and eighth phase signals coming from nodes G and H, are supplied by AND-INVERTs 417, 423, 419, and 425 of nodes from the first and second primary and secondary phase generators 210A, 210B, 220A and 220B respectively. The fifth and sixth phase signals from nodes G and H are small instead of the half cycle, because these signals should not be recharging the first and second main pump capacitors 486 and 492 while they are being pre-booted by the first and second pre-boot capacitors 462 and 464, otherwise the pre-boot charges will be shunted to V_{cc}.